

### Abstract

A MOS semiconductor device includes n<sup>-</sup>-type surface regions, which are extended portions of an n<sup>-</sup>-type drift layer 12 extended to the surface of the semiconductor chip. Each n<sup>-</sup>-type surface region 14 is shaped with a stripe surrounded  
5 by a p-type well region. The surface area ratio between n<sup>-</sup>-type surface regions 14 and p-type well region 13 including an n<sup>+</sup>-type region 15 is from 0.01 to 0.2. The MOS semiconductor device further includes, in the breakdown withstanding region thereof, a plurality of guard rings, the number of which is equal to or more than the number n  
calculated from the following equation  $n = (\text{Breakdown voltage } V_{br} \text{ (V)})/100$ , and the  
10 spacing between the adjacent guard rings is set at 1  $\mu\text{m}$  or less.